

EX – 9930

***16 Ch. Opto-isolated Digital
Input Module***

OPERATING GUIDE

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GENERAL DESCRIPTION

The EX-9930 opto-isolated input PC/104 module is designed for monitoring digital input status. It provides 16 channels of input to detect ON/OFF, OPEN/CLOSE signals and has interrupt capability on its first channel. The input range is from 5V to 24V suitable for many applications. Also the isolation voltage is up to 1000 Vrms from the input end to the host. This feature causes voltage spikes that often occur in harsh industrial environments to be safely isolated from the computer.

Features

- 16 channels opto-isolated input
- Isolation up to 1000 Vrms
- Filter circuit included
- Wide input range

Applications

- Industrial ON/OFF monitoring
- Limit switch monitoring
- Valve/Solenoid monitoring

Specifications

Input

Opto-isolator	PC814 or equivalent
Number of Channels	16
Voltage Range	$\pm 5V - \pm 24V$ (logic 1 output)
Current Limit Resistor	$1.2k\Omega, 0.5W$
Max Current	$\pm 50mA$
Connector	50-pin mating connector

Power Requirements

+5VDC	400mA
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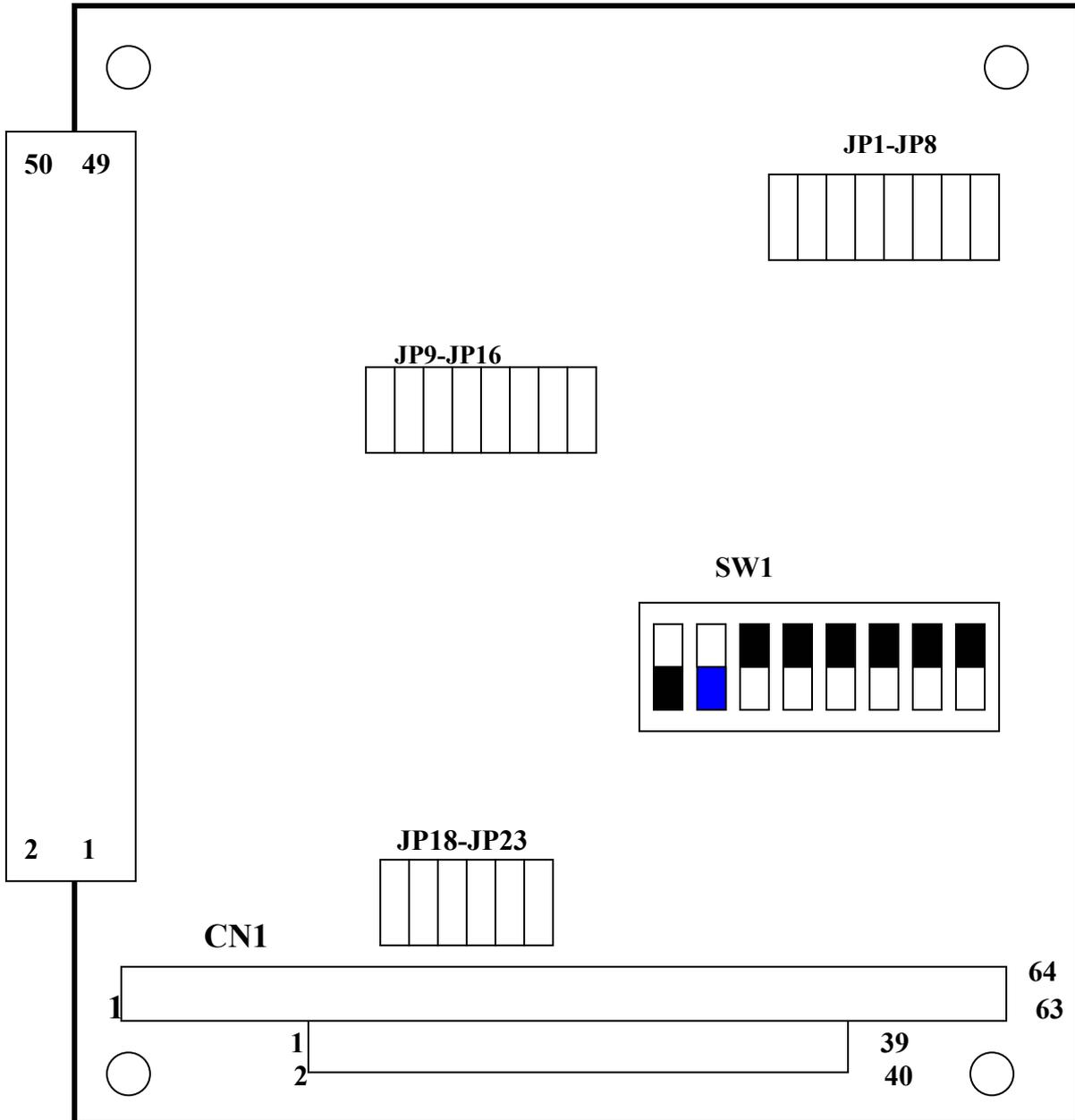
Physical/Environmental

Dimension	95mm x 90mm
Weight	80g
Operating Temperature Range	0 to 50°C
Storage Temperature Range	- 25 TO + 85°C
Relative Humidity	0 TO 90%, non-condensing

MODULE CONFIGURATION AND INSTALLATION

Location Diagram

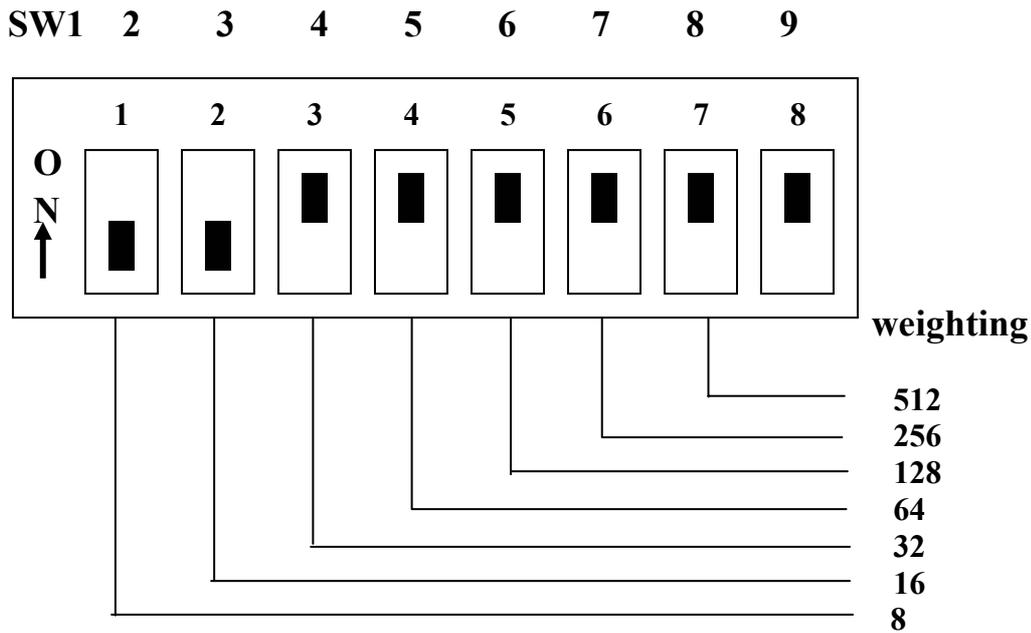
Refer to the following location diagram for help locating components needed during installation of the EX-9930 module.



DIP Switch setting

EX-9930 occupies four consecutive I/O port spaces. The I/O port addresses are set via a DIP switch labeled SW1. Set the DIP switch to correct address and avoid conflicting with other devices. Valid addresses are from 200 Hex to 3F8 Hex. The following figure is the default setting; 300 Hex.

BASE ADDRESS SWITCH SETTING



$$\begin{aligned} \text{Base Address} &= 512 + 256 = 768 \text{ (Decimal)} \\ &= 300 \text{ (Hexadecimal)} \end{aligned}$$

I/O PORT RANGE	DIP SWITCH POSITION							
HEXADECIMAL	1	2	3	4	5	6	7	8
	A2	A3	A4	A5	A6	A7	A8	X
200 – 203	0	0	0	0	0	0	1	0
204 – 207	1	0	0	0	0	0	1	0
208 – 20B	0	1	0	0	0	0	1	0
20C – 20F	1	1	0	0	0	0	1	0
.	.			.			.	
.	.			.			.	
220 – 223	0	0	0	1	0	0	1	0
.	.			.			.	
.	.			.			.	
300 – 303(*)	0	0	0	0	0	1	1	0
.	.			.			.	
.	.			.			.	
3F8 – 3FB	0	1	1	1	1	1	1	0
3FC – 3FF	1	1	1	1	1	1	1	0

0 = ON, 1 = OFF

(*) : Factory default setting

Jumper Setting

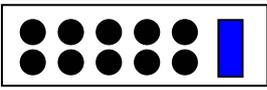
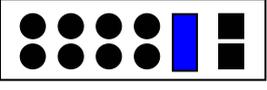
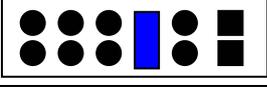
JP1 – JP8 : These are filter control jumpers used to enable or disable channel 0 through channel 7 filterings. If jumper cap is installed, the filter is turn on when the 3-dB frequency is located at about 50 Hz.

Channel	0	1	2	3	4	5	6	7
Corresponding Jumper	JP1	JP2	JP3	JP4	JP5	JP6	JP7	JP8

JP9 – JP16 : These are filter control jumper used to enable or disable channel 8 through channel 15 filterings. If jumper cap is installed, the filter is turn on where the 3-dB frequency is located at about 50Hz

Channel	8	9	10	11	12	13	14	15
Corresponding Jumper	JP8	JP9	JP10	JP11	JP12	JP13	JP14	JP15

JP18 – JP23 : These are interrupt request output selection jumpers. The following table shows jumper cap position versus IRQ channel relationship. Remember only channel 0 has interrupt capability.

JP18 – JP23 Jumper Cap Position	Description
	IRQ2 Selected
	IRQ3 Selected
	IRQ4 Selected
	IRQ5 Selected
	IRQ6 Selected
	IRQ7 Selected

Connector Pin Assignment

JP1

NAME	PIN	PIN	NAME
DI0	1	2	DI8
-DI0	3	4	-DI8
GND	5	6	GND
DI1	7	8	DI9
-DI1	9	10	-DI9
GND	11	12	GND
DI2	13	14	DI10
-DI2	15	16	-DI10
GND	17	18	GND
DI3	19	20	DI11
-DI3	21	22	-DI11
GND	23	24	GND
DI4	25	26	DI12
-DI4	27	28	-DI12
GND	29	30	GND
DI5	31	32	DI13
-DI5	33	34	-DI13
GND	35	36	GND
DI6	37	38	DI14
-DI6	39	40	-DI14
GND	41	42	GND
DI7	43	44	DI15
-DI7	45	46	-DI15
+12V	47	48	+12V
+12V	49	50	+12V

PIN	SIGNAL NAME	DESCRIPTION
1,7,13,19,25 31,37,43	DI0 – DI7	The lower eight positive digital input channels. These pin are labeled as positive.
3,9,15,21,27, 33,39,45	-DI0 - -DI7	The lower eight negative digital input channels. These pin are labeled as negative.
2,8,14,20,26, 32,38,44	DI8 – DI15	The upper eight positive digital input channels. These pin are labeled as negative.
4,10,16,22,28 , 34,40,46	-DI8 - -DI15	The upper eight negative digital input channels. These pin are labeled as negative.
47,48,49,50	+12V	+12V PC bus power
5,6,11,12,17, 18,23,24,29 30,35,36,41, 42	GND	PC ground.

NOTE: Be careful when using the +12V power as it is directly from PC bus. Users are suggested to use external power source for data safety reasons.

Module Installation

The EX-9930 PC/104 module is shipped with protective electrostatic cover. When unpacking, touching the module electrostatically shielded packaging with the metal frame of your computer to discharge the accumulated static electricity prior to touching the module.

Following description summarizes the procedures for installing the EX-9930:

WARNING

TURN OFF the PC and all accessories connected to the PC whenever installing or removing any peripheral board including the EX-9930 module.

Installation procedures;

- 1. Turn off the system power.**
- 2. Unplug all power cords.**
- 3. Remove the case cover if necessary.**
- 4. Remove the top module if it is a non-stackthrough module.**
- 5. Put the EX-9930 module in line with top present module as described in PC/104**
MECHANICAL SPECIFICATION.
- 6. Install four spacers if necessary.**
- 7. Connect cable if necessary.**
- 8. Crush between the module until inside distance is SPACER's height (0.6") Restore all the screws.**
- 9. Repeat step 6 until all module are set into position.**
- 10. Connect cable to EX-9930 if necessary.**
- 11. Replace the case cover and connect all the necessary cables.**
- 12. Turn on the system power.**

REGISTER DESCRIPTION

I/O Map

The EX-9930 occupies 4 consecutive addresses in I/O address space, but only two of the I/O addresses are actually used. The 16 individually opto-isolated inputs are read as two bytes of data.

The following table shows the two 8-bit digital input registers:

Base Address + 0

Bit No.	7	6	5	4	3	2	1	0
Digital Input	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

This is a read only register for the lower digital input byte data. The write action will not have any effect.

Base Address + 1

Bit No.	7	6	5	4	3	2	1	0
Digital Input	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

This is a read only register for the higher digital input byte data. The write action will not have any effect.

PROGRAMMING

Programming the EX-9930 is very simple. It can be easily accomplished using direct I/O instructions of whatever application languages. In this section an example in BASIC is given.

Let's assume the base address is 300Hex, the programming is as follows:

```
BASE = &H300
```

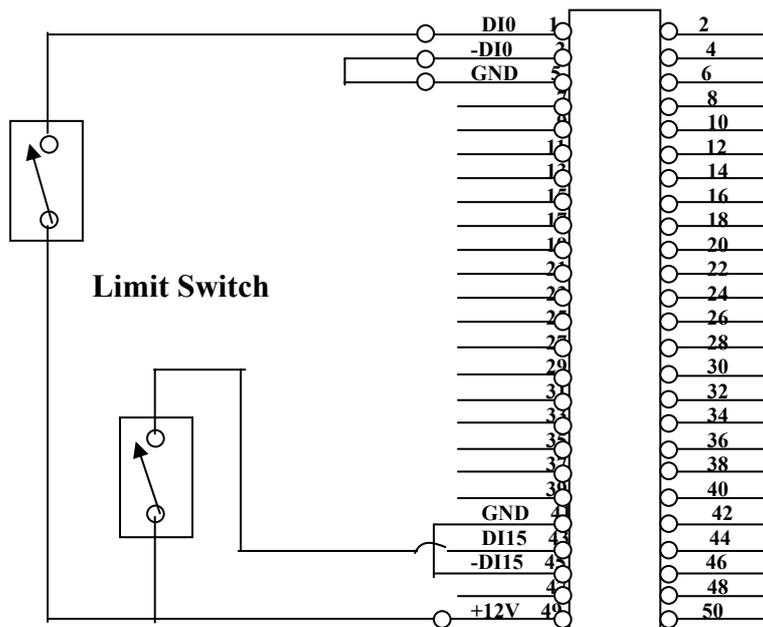
```
X1% = INP (BASE)
```

```
IF X1%&1 THEN PRINT "Channel 0 is ON" ELSE PRINT "Channel 0 is OFF"
```

```
X2% = INP (BASE + 1)
```

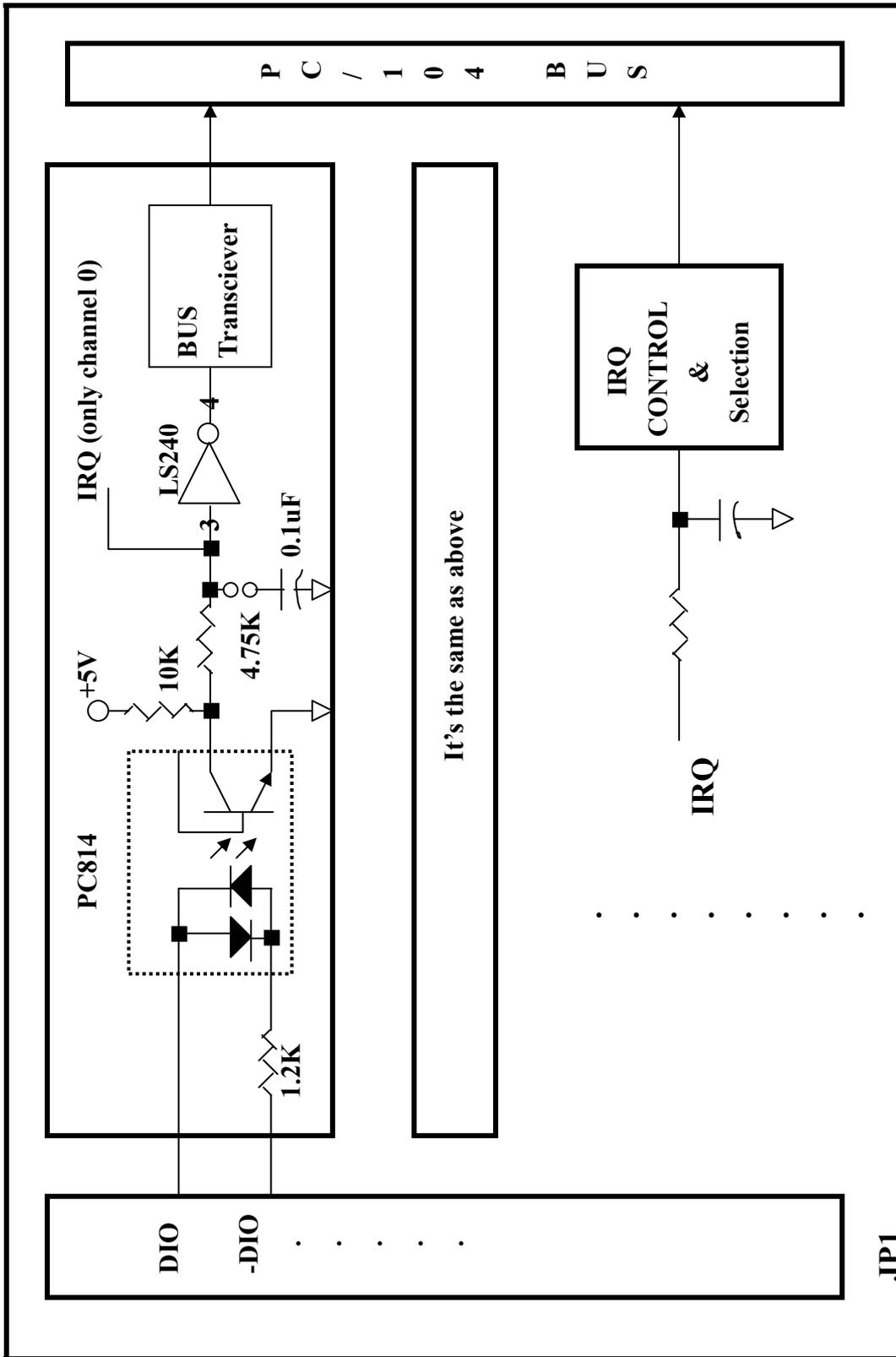
```
IF X2%&1 THEN PRINT "Channel 8 is ON" ELSE PRINT "Channel 8 is OFF"
```

WIRING: This is the most simplest way to detect a switch whether it is close or open.



WARNING: *The +12V PC power had better not to be effected by outside world. otherwise it may cause the PC to fail accessing data to hard-disk!*

BLOCK DIAGRAM



APPENDIX A

PC I/O PORT MAPPING

I/O PORT ADDRESS RANGE	FUNCTION
000 – 1FF	PC reserved
200 – 20F	Game controller (Joystick)
278 – 27F	Second parallel printer port (Lpt2)
2E1	GPIB controller
2F8 – 2FF	Second serial port (COM2)
320 – 32F	Fixed disk (XT)
378 – 37F	Primary parallel printer port (LPT1)
380 – 38F	SDLC communication port
3B0 – 3BF	Monochrome adapter/printer
3C0 – 3CF	EGA, reserved
3D0 – 3DF	Color/graphics adapter
3F0 – 3F7	Floppy disk controller
3F8 – 3FF	Primary serial port (COM1)

APPENDIX B

SUMMARY OF INTERRUPT LEVELS

Interrupt Level	Usage
NMI	Parity, AT Channel Check
IRQ0	Interval Timer 1, Counter 0 OUT
IRQ1	Keyboard Controller
IRQ2	Reserved (XT) Cascade Interrupts from IRQ8 to IRQ15(AT)
IRQ3	Serial Port # 2
IRQ4	Serial Port # 1
IRQ5	Hard Disk(XT) Parallel Port # 2(AT)
IRQ6	Floppy Disk
IRQ7	Parallel Port # 1
IRQ8	Real Timer Clock(AT)
IRQ9	Re-directed to IRQ2(AT)
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	Unassigned
IRQ13	Coprocessor Error
IRQ14	Hard Disk
IRQ15	Unassigned

APPENDIX C

PC/104 MECHANICAL SPECIFICATIONS

PC/104 General Description

While the PC and PC/AT architectures have become extremely popular in both general purpose (desktop) and dedicated (non-desktop) applications, its use in embedded microcomputer applications has been limited due to the large size of standard PC and PC/AT motherboards and expansion cards. PC/104 module can be of two bus types, 8 bit and 16 bit, which correspond to the PC and PC/AT buses, respectively.

Besides bus option, there are stackthrough and non-stackthrough difference. The stackthrough version provides a self-stacking PC bus. It can be placed any where in a multi-module stack. The non-stackthrough version offers minimum thickness, by omitting bus stackthrough pins. It must be positioned at one end of a stack.

For convenience . the EX-9930 is equipped with stackthrough version only. (NOTE : For safety, you are suggested to cut bus stackthrough pins of the last module on condition; that you are sure you won't add/plug any module to the module stack in the future.)

The following sections provide the mechanical and electrical specification for a compact version of the PC/AT bus, optimized for the unique requirements of embedded systems applications. The specification is herein referred to as "PC/104". Based on the 104 signal contacts on the two bus connectors (64 pin on CN1 plus 40 pin on CN2).

Module Dimensions

PC/104 modules can be of two bus types, 8-bit and 16-bit, which correspond to PC and PC/AT buses, respectively.